**GPIO Module Description Document**

**1. General-Purpose GPIO**

The chip provides three groups of GPIOs: GPIOA, GPIOB, and GPIOC.In addition to serving as standard GPIOs, these pins can also be multiplexed for other functions such as FUART, SPI, PWM, etc.

* 1. **Internal Structure Diagram**

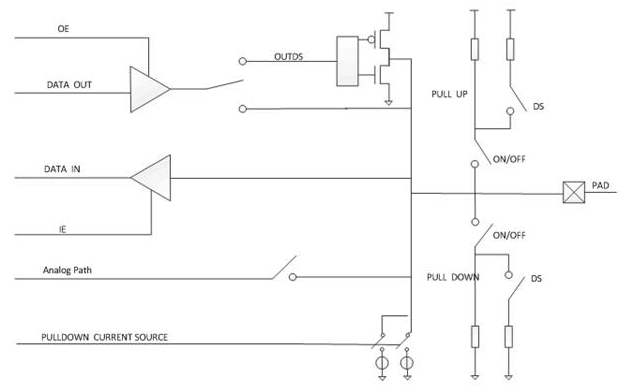


Figure 1 GPIO Internal Structure Diagram

Each GPIO port is controlled by several registers, allowing it to be configured into multiple modes via software.Figure 1 is the GPIO internal structure diagram.OE is the Output Enable register, DATA OUT is the Output Data register, OUTDS is the Output Drive Capability Configuration register, IE is the Input Enable register, DATA IN is the Input Data register, Analog Path is the analog channel, PULLDOWN CURRENT SOURCE is the Pulldown Current Source register, PULL UP/PULL DOWN is the Pull-up/Pull-down register, DS is the Pull Strength Configuration register, and PAD is the package pin.

Table 1 — GPIO Configuration Table , Table 2 — GPIO Pull-up/Pull-down Configuration Table,Table 3 — GPIO Pulldown Current Source Output Current Values (Note 3)

Table 1 GPIO Configuration Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Configuration Mode** | **State** | **OE** | **IE** | **OUTDS** | **DS** | **PU** | **PD** |
| Digital Output | Strong Drive Output (Note 1) | 1 | 0 | 1 | \* | \* | \* |
| Weak Drive Output | 1 | 0 | 0 | \* | \* | \* |
| Strong Pull-Up/Pull-Down Output (Note 2) | 1 | 0 | \* | 1 | \* | \* |
| Weak Pull-Up/Pull-Down Output | 1 | 0 | \* | 0 | \* | \* |
| Digital Input | Strong Pull-Up/Pull-Down Input | 0 | 1 | 0 | 0 | \* | \* |
| Weak Pull-Up/Pull-Down Input | 0 | 1 | 0 | 1 | \* | \* |
| Analog Input | Analog Input | 0 | 0 | \* | \* | 0 | 1 |

Note 1: OUTDS=0 : 8mA (VOL=0.4V, VOH=2.4V)；OUTDS=1 : 24mA  (VOL=0.4V, VOH=2.4V)

Note 2: DS = 1： 70uA；  DS = 0：20uA

Table 2 GPIO Pull-up/Pull-down Configuration Table

|  |  |  |
| --- | --- | --- |
| **Configuration Functions** | **PU** | **PD** |
| Pull-Up | 0 | 0 |
| Analog Channel | 0 | 1 |
| No Pull-Up, No Pull-Down | 1 | 0 |
| Pull-Down | 1 | 1 |

Table 3 GPIO Pulldown Current Source Output Current Values (Note 3)

|  |  |  |
| --- | --- | --- |
| **Dropped current source current value (mA)** | **PULLDOWN1** | **PULLDOWN2** |
| 0 | 0 | 0 |
| 1.7 | 1 | 0 |
| 2.4 | 0 | 1 |
| 4.1 | 1 | 1 |

Note 3: Test conditions: PU = 1，PD = 0，IE = 1，OE = 0，DS = 0，OUTDS = 0

**1.2. Functional Description**

GPIOs can be configured as **digital input/output**, **analog input**, **interrupt**, or **multiplexed** functions.

**Table 4** — Default GPIO Power-on State

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **Pin Type** | **Default Pull-Down State** | **Default Level** |
| GPIOA[1：0] | Anti-Bounce GPIO | Pull-Down | L |
| GPIOA[10：2] | Normal GPIO | Pull-Up | H |
| GPIOA[12：11] | Anti-Bounce GPIO | Pull-Down | L |
| GPIOA[21：13] | Normal GPIO | Pull-up | H |
| GPIOA[25：22] | Normal GPIO | No pull up/No pull down | L |
| GPIOA[31：26] | Normal GPIO | Pull-up | H |
| GPIOB[31:0] | Normal GPIO | Pull-up | H |
| GPIOC[12：0] | Normal GPIO | Pull-up | H |
| GPIOC13 | Normal GPIO | Pull-Down | L |
| GPIOC14 | Normal GPIO | Pull-up | H |

**1.2.1. Digital Input Function**

When a GPIO is used as a digital input pin:

 Can be configured as pull-up, pull-down, or no pull.

 Can be configured as strong pull or weak pull.

When configured for pull-up or pull-down, it can be set to 70 µA strong pull or 20 µA weak pull as needed. The chip’s default power-on state is a 20 µA weak pull.

 Each GPIO’s digital input status can be read.

**1.2.2. Digital Output Function**

When a GPIO is used as a digital output pin:

  Can output high level or low level.

  Can be configured as pull-up, pull-down, or floating.

  Can be configured as strong pull or weak pull.

When configuring GPIO as pull-up or pull-down, it can be set to a strong pull-up state of 70uA or a weak pull-up/pull-down state of 20uA according to actual requirements. The default state upon power-on is a weak pull-up state of 20uA.

  Can be configured as strong drive or weak drive.

When configuring GPIO as output pins, you can configure GPIO as either a strong drive output state or a weak drive output state based on the actual application requirements. In the strong drive output state, the GPIO pins can output a drive current of up to 24mA, while in the weak drive output state, the GPIO pins can output a drive current of 8mA. The default state upon power-on is the weak drive current output.

**1.2.3. Analog Input Function**

When a GPIO is used as an analog input pin:

 Pull-up/pull-down configuration is not allowed.

 Can be used by the ADC module.

 Can be used by the USB PHY module.

 Can be used by the LCD segment display module.

 Can be used by Touch Key In.

 Can be used by VCOM.

 Can be used by FM IN.

**1.2.4. Interrupt Function**

All three GPIO groups can be used for GPIO interrupts.To use GPIO interrupts, the pin must first be configured as a digital input.

 GPIO interrupts can be enabled or disabled.

 Trigger polarity can be configured as rising edge or falling edge.

Default power-on trigger polarity is falling edge, but it can be reconfigured as needed.

 You can read the interrupt status of each GPIO pin.

You can read the interrupt status of each GPIO, but the interrupt status flag needs to be cleared through software.

**1.2.5. Multiplexed Function**

In addition to its GPIO functionality, the GPIO can also be mapped to other functions. The corresponding pins can be mapped according to actual functional requirements. After the chip is powered on, except for the GPIO pin corresponding to SW, which is mapped to SW, all other GPIO pins default to general-purpose mode. When the GPIO can be mapped to a multiplexed mode, the following options are available:

Can be mapped to 4 groups of SPIM interface pins.

Can be mapped to 3 groups of Fuart receive/transmit interface pins.

Can be mapped to 4 groups of Buart receive/transmit interface pins.

Can be mapped to 3 groups of Buart Rts interface pins.

Can be mapped to 3 groups of Buart Cts interface pins.

Can be mapped to 4 groups of SD interface pins.

Can be mapped to 1 group of LCD interface pins.

Can be mapped to 2 groups of PWC pins.

Can be mapped to 3 groups of Ir pins.

Can be mapped to 2 groups of Fshc interface pins.

Can be mapped to 1 group of SDRAM interface pins.

Can be mapped to 3 groups of 32 kHz CLK output pins.

Can be mapped to 3 groups of 12 MHz/16 MHz CLK output pins.

Can be mapped to 3 groups of PCM interface pins.

Can be mapped to 3 groups of I2S interface pins.

Can be mapped to 4 groups of Mclk pins.

Can be mapped to 1 group of SW interface pins.

Can be mapped to 1 group of SPIS interface pins.

Can be mapped to 1 group of CTS (Capacitive Touch Sensor) comparison signal pins.

After being mapped to other functions, if you need to remap them back to general-purpose GPIO functionality, you must disable the pin's multiplexing mapping; otherwise, the GPIO cannot be used directly. Additionally, GPIO pins may be multiplexed by multiple modules, so it is essential to ensure that at any given time, a single GPIO pin can only be used for one function.

* 1. **Interface File Brief Description**

**1.3.1. Macro Definitions Description**

In the gpio.h file, all macro definitions and type definitions required for GPIO interface functions are defined.Below is an example using GPIOA:

GPIO\_A\_IN: GPIOA input data register index.

GPIO\_A\_OUT: GPIOA output data register index.

GPIO\_A\_IE: GPIOA input enable register index.

GPIO\_A\_OE: GPIOA output enable register index.

GPIO\_A\_DS: GPIOA pull-up/pull-down drive strength register index.

GPIO\_A\_OUTDS: GPIOA output drive capability register index.

GPIO\_A\_PU: GPIOA pull-up register index.

GPIO\_A\_PD: GPIOA pull-down register index.

GPIO\_A\_PULLDOWN1 / GPIO\_A\_PULLDOWN2: GPIOA pulldown current source configuration register index.

GPIOA1: Used with GPIOA port registers, represents BIT1 of the register.

GPIO\_A\_INT: GPIOA interrupt register index.

GPIO\_NEG\_EDGE\_TRIGGER: GPIO interrupt trigger mode – falling edge.

GPIO\_POS\_EDGE\_TRIGGER: GPIO interrupt trigger mode – rising edge.

#define SET\_C11\_ANALOG\_IN() \

GpioClrRegBits(GPIO\_C\_PU, GPIOC11), \

GpioSetRegBits(GPIO\_C\_PD, GPIOC11), \

GpioClrRegBits(GPIO\_C\_IE, GPIOC11), \

GpioClrRegBits(GPIO\_C\_OE, GPIOC11)

Configures GPIOC11 as an analog input.

 #define SET\_C12\_ANALOG\_IN() \

GpioClrRegBits(GPIO\_C\_PU, GPIOC12), \

GpioSetRegBits(GPIO\_C\_PD, GPIOC12), \

GpioClrRegBits(GPIO\_C\_IE, GPIOC12), \

GpioClrRegBits(GPIO\_C\_OE, GPIOC12)

Configures GPIOC12 as an analog input.

 #define SET\_C13\_ANALOG\_IN() \

GpioClrRegBits(GPIO\_C\_PU, GPIOC13), \

GpioSetRegBits(GPIO\_C\_PD, GPIOC13), \

GpioClrRegBits(GPIO\_C\_IE, GPIOC13), \

GpioClrRegBits(GPIO\_C\_OE, GPIOC13)

Configures GPIOC13 as an analog input.

 #define SET\_C14\_ANALOG\_IN() \

GpioClrRegBits(GPIO\_C\_PU, GPIOC14), \

GpioSetRegBits(GPIO\_C\_PD, GPIOC14), \

GpioClrRegBits(GPIO\_C\_IE, GPIOC14), \

GpioClrRegBits(GPIO\_C\_OE, GPIOC14)

Configures GPIOC14 as an analog input.

**GPIO Special Functions**

**1.4. Reverse Current Protection Function**

The chip provides three groups of GPIOs, namely GPIOA, GPIOB, and GPIOC. Among them, the four GPIO pins GPIOA0, GPIOA1, GPIOA11, and GPIOA12, in addition to serving as ordinary GPIOs, also have the function of preventing backflow. Anti-backflow GPIO refers to the fact that when the system is powered off and there is external voltage, no current will flow into the chip through these pins. This pin can be used in some applications that require a relatively high voltage field.

The advantage of anti-backflow lies in that it can not only effectively prevent current backflow when the chip is PowerDown, but also effectively prevent current backflow when the chip is PowerOn if the external voltage is too high. When using the anti-backflow function, the Charge Pump module needs to be enabled. This function has been enabled by default in the boot code provided by Shanjing.

**1.5. Charging Indicator Function**

In addition to being a common GPIO with anti-backflow function, GPIOA0 also has the function of charging indication. The charging indication function is implemented using anti-backflow IO, with the aim of enabling the chip to still activate the charging indication function after PowerDown.

The charging indication function can achieve:

 The on-off of the pull-down current source is periodically (with adjustable frequency) controlled by the internal LED circuit, thereby achieving the charging flashing function. Flickering frequency range: 1HZ to 16HZ.

 When the charging is complete, that is, when the VIN is higher than 4.15V, the charging is over. The software can configure the polarity to make the pull-down current source always on or always off, thereby showing that the indicator light remains on or off after the charging is completed.

 GPIOA0 can be configured to enable the hardware input constant current source as: 1.7mA, 2.4mA, 4.1mA.